

FIGURE 1

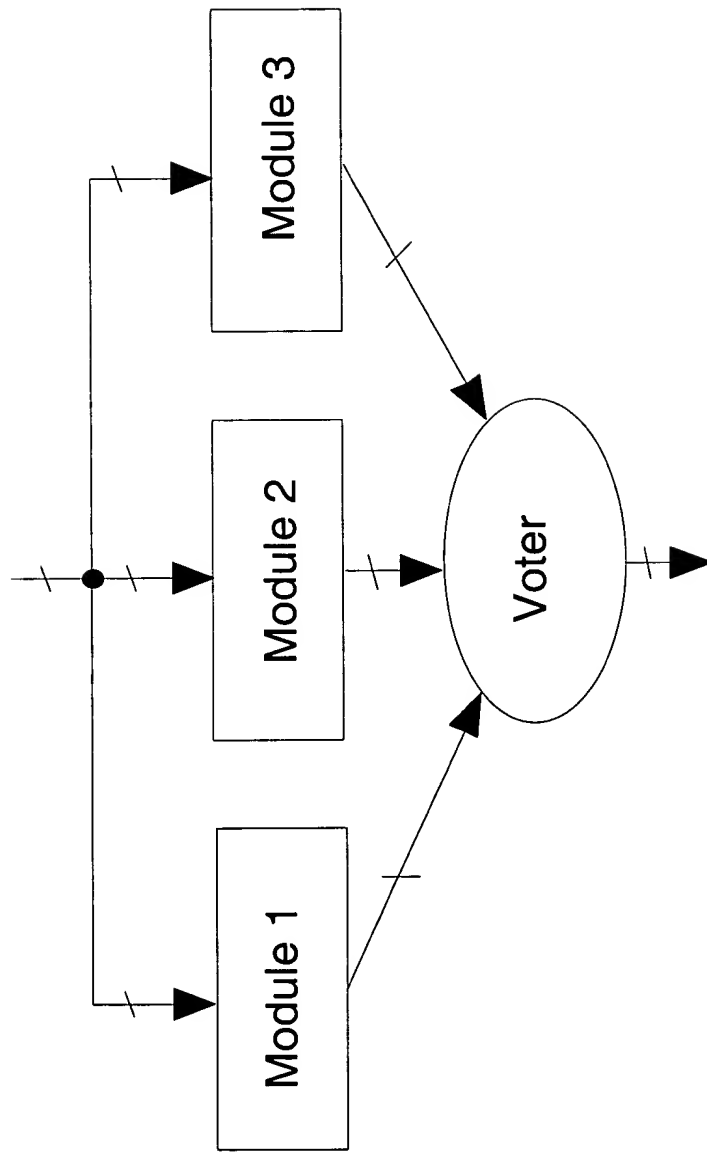


Figure 2 is a block diagram of a logic circuit. The circuit has three inputs: Z_1^1 , Z_1^2 , and Z_1^3 . The inputs Z_1^1 and Z_1^2 are connected to the inputs of three AND gates. The output of the first AND gate is connected to the input of an adder. The output of the second AND gate is connected to the input of an adder. The output of the third AND gate is connected to the input of an adder. The output of the adder is Z_1 .

FIGURE 2

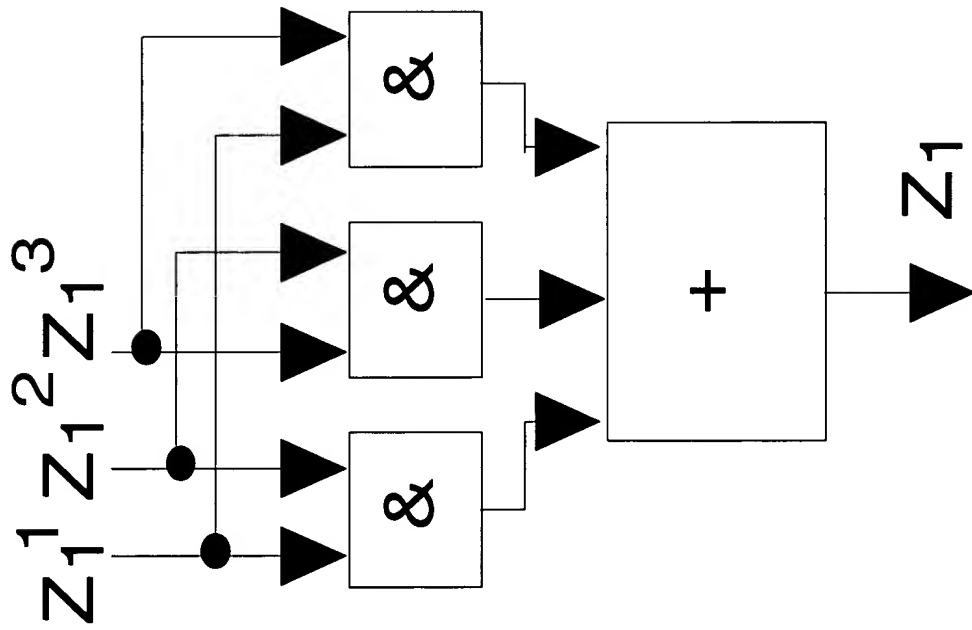
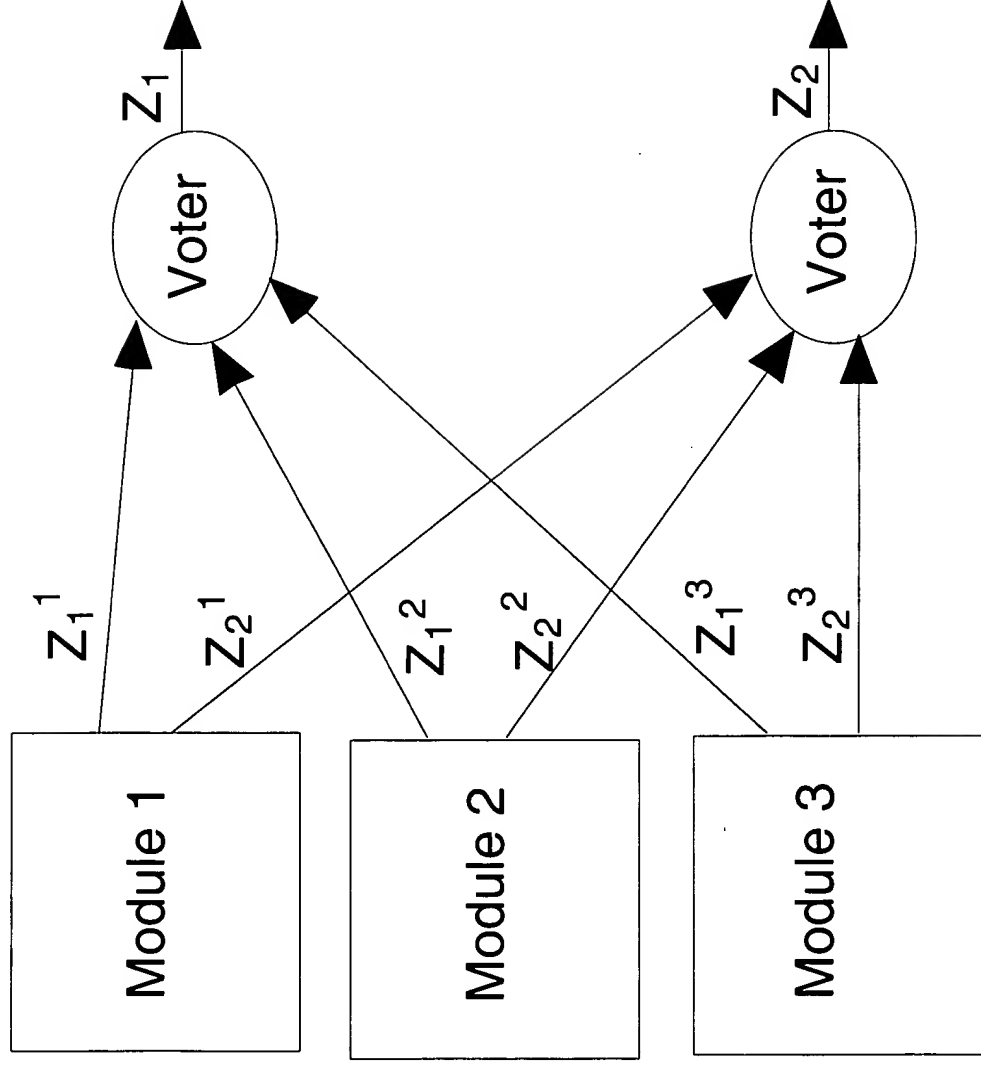


FIGURE 3



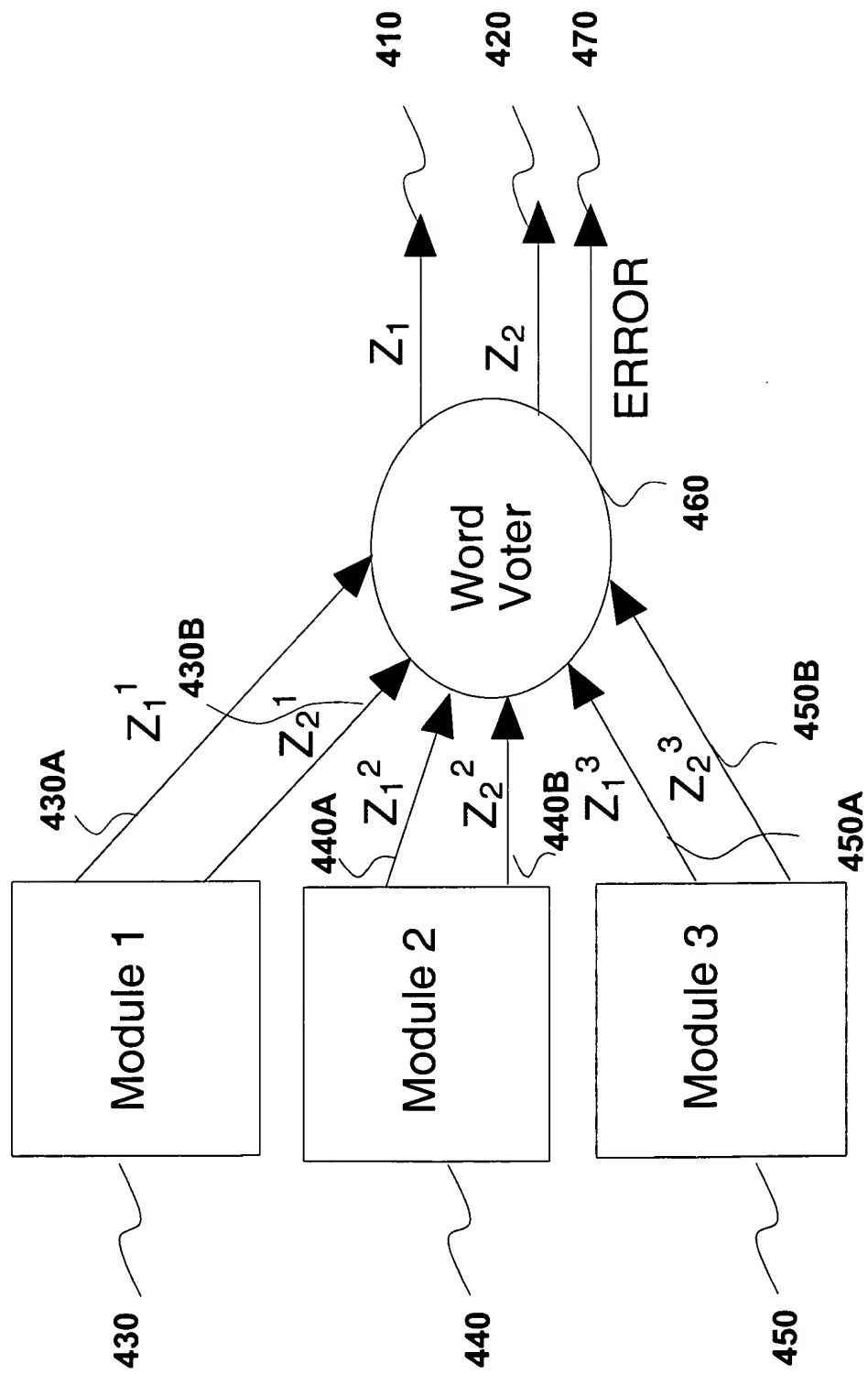


FIGURE 5

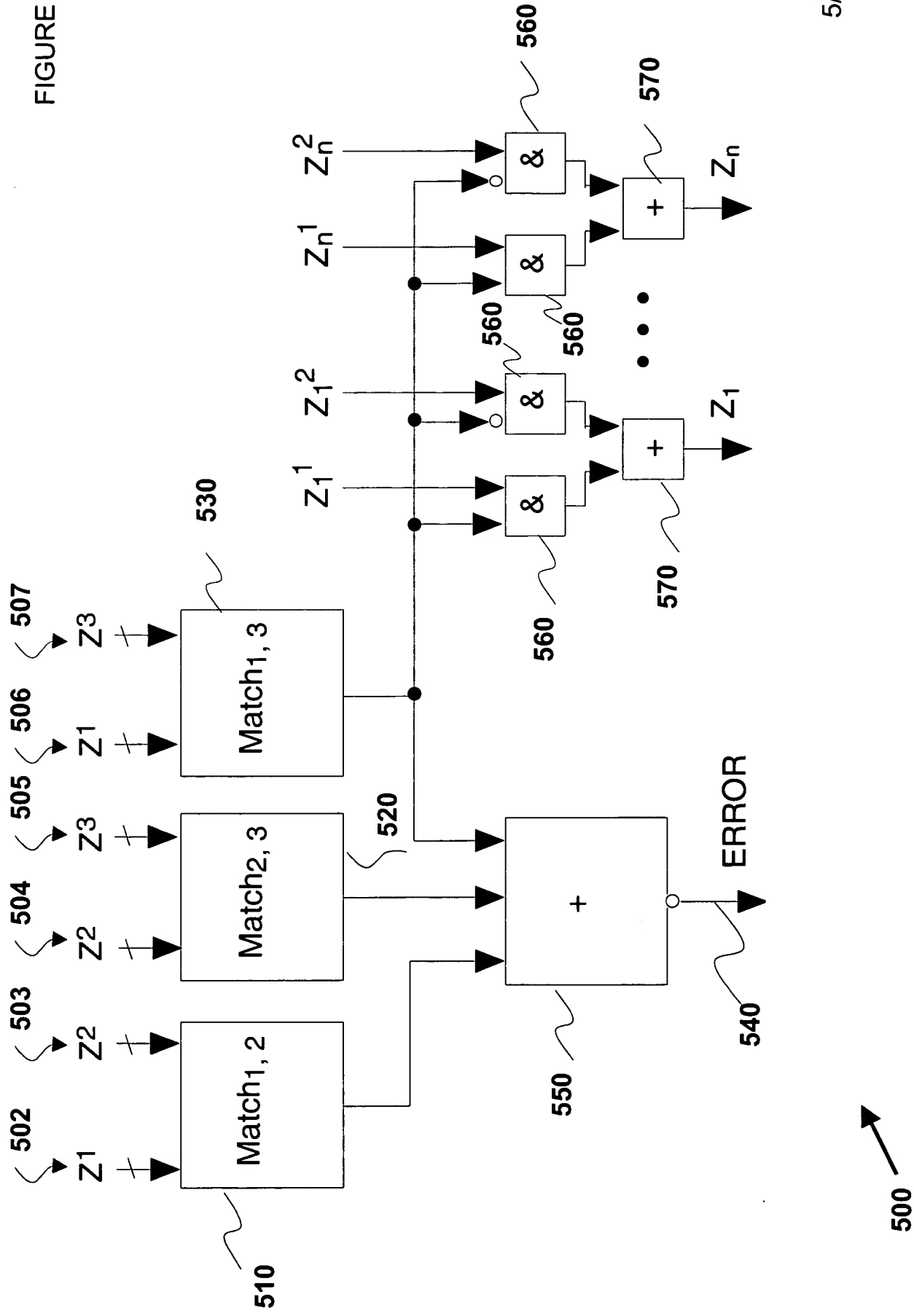


FIG. 6 is a block diagram of a match circuit 600. The match circuit 600 is configured to determine whether a first input vector Z_1 matches a second input vector Z_n . The match circuit 600 includes a plurality of XOR gates 620 and an AND gate 560. The first input vector Z_1 is provided to the match circuit 600 via inputs Z_{1i} and Z_{1j} . The second input vector Z_n is provided to the match circuit 600 via inputs Z_{ni} and Z_{nj} . Each XOR gate 620 receives a pair of inputs Z_{1i} and Z_{ni} (or Z_{1j} and Z_{nj}). The output of each XOR gate 620 is connected to the AND gate 560. The AND gate 560 produces a match signal $Match_{i,j}$ when all corresponding inputs of the first and second input vectors match.

FIGURE 6

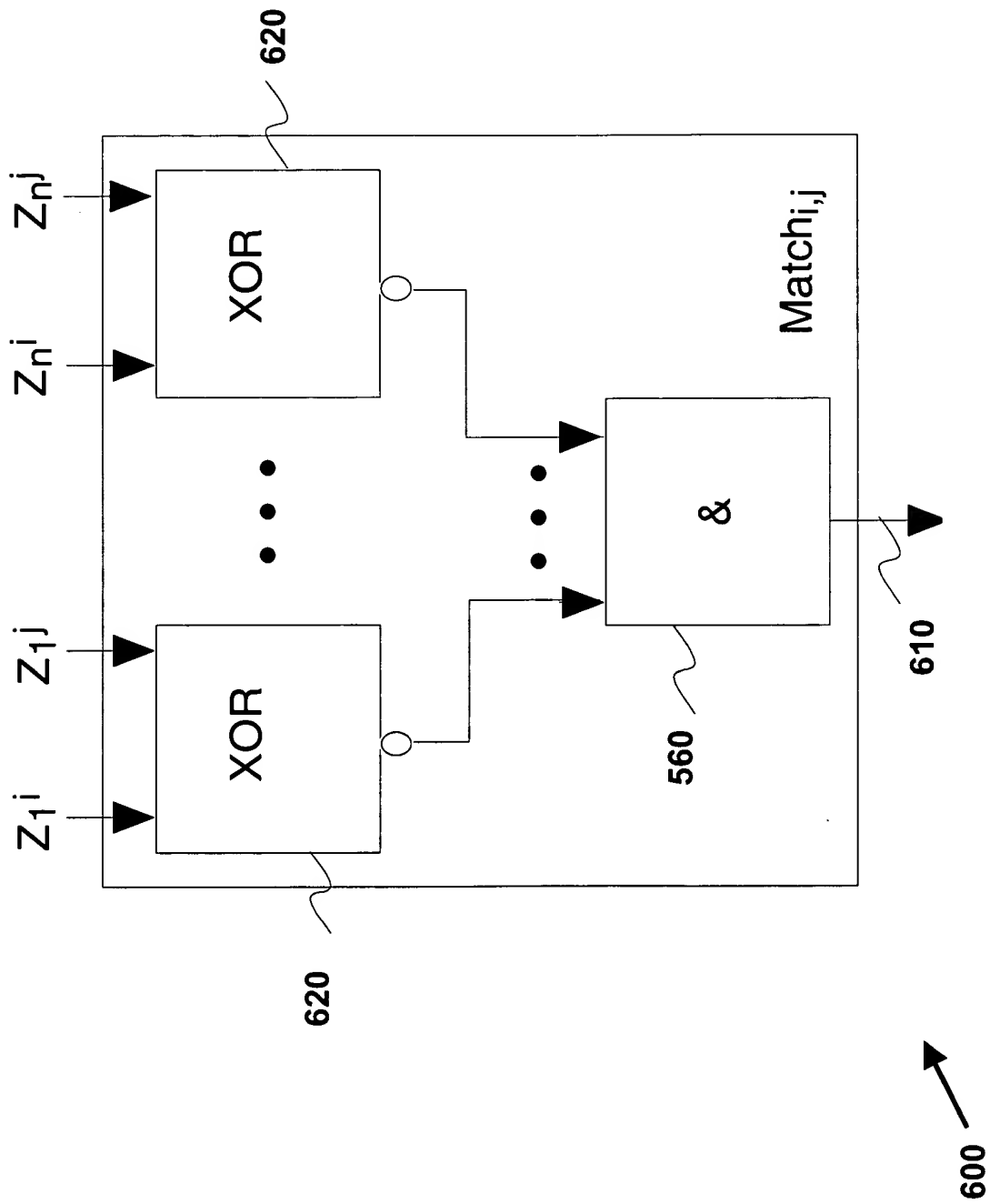


FIGURE 7

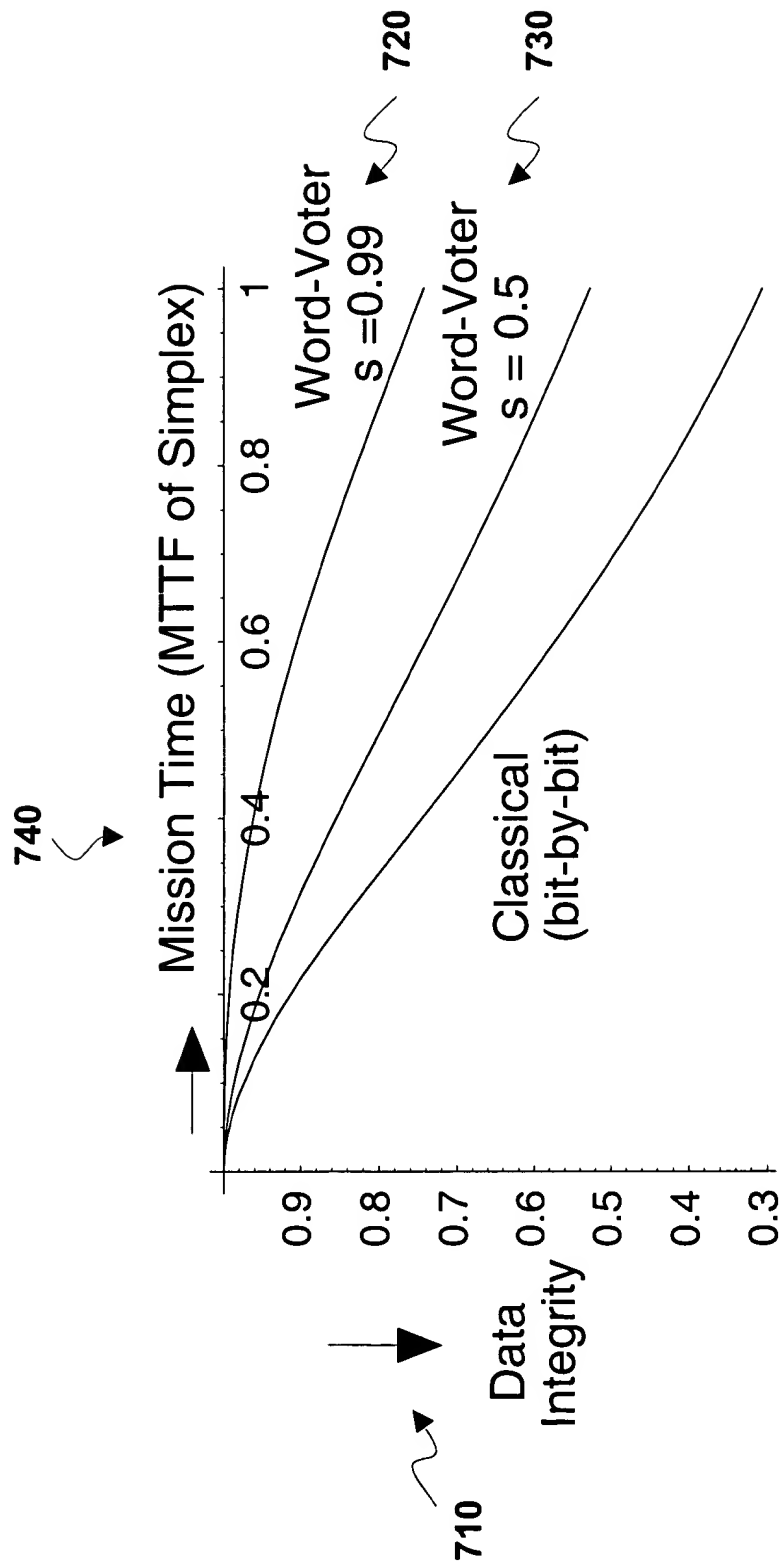


FIGURE 8

